

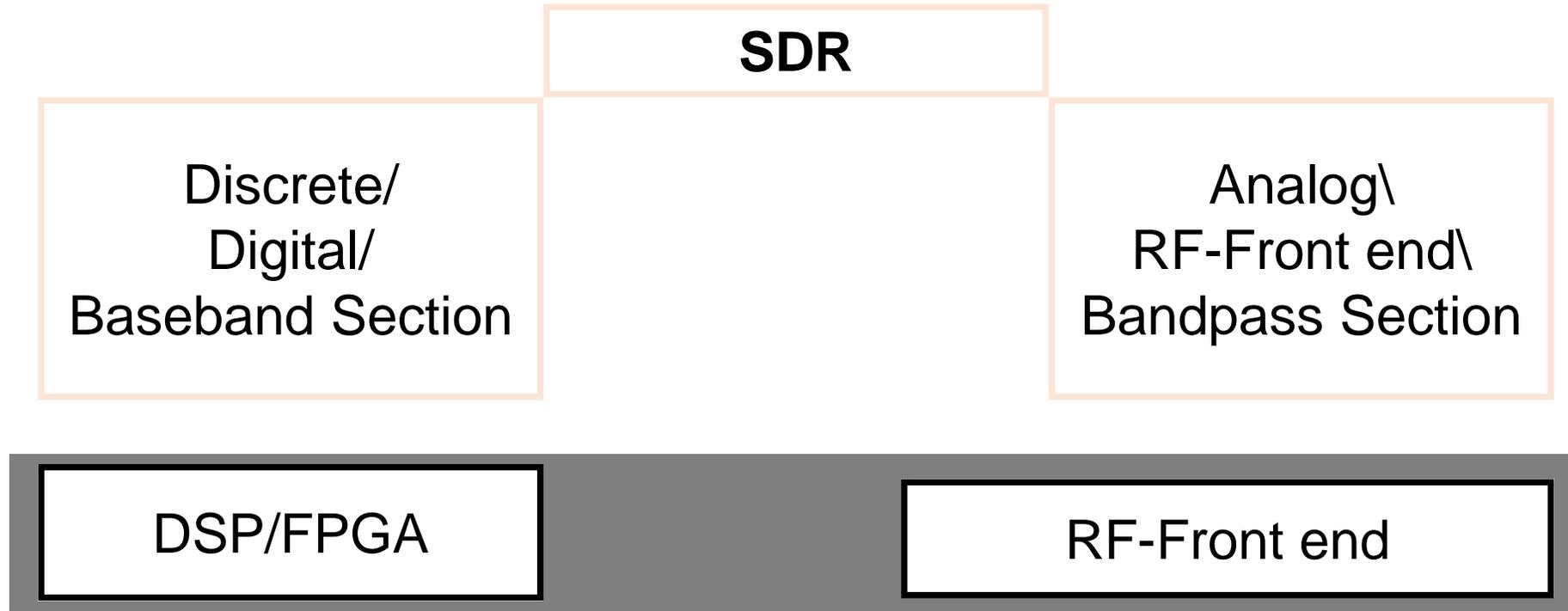
Fundamentals of SDR:RAHSDR480

Module-2:SDR Hardware Architecture

RAHSDR480_L02_P01_R01:SDR Hardware



SDR Hardware



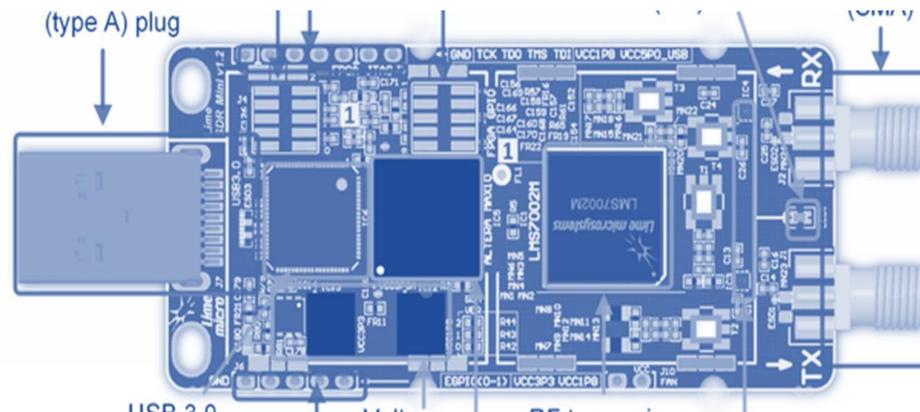
Discrete/
Digital/
Baseband Section

SDR

Analog/
RF-Front end/
Bandpass Section

DSP/FPGA

RF-Front end



Heterodyne

Homodyne



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CONT....

Receiver Selectivity

- Ability of a receiver to select a desired signal in the presence of other unwanted signals.

Receiver Sensitivity

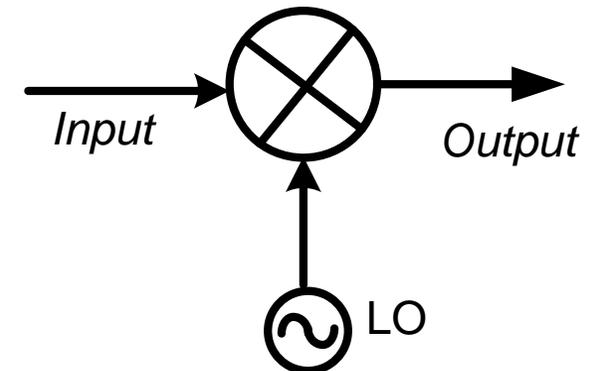
- Lowest signal power level at the input of a receiver which guarantees proper working of a wireless receiver.



CONT....

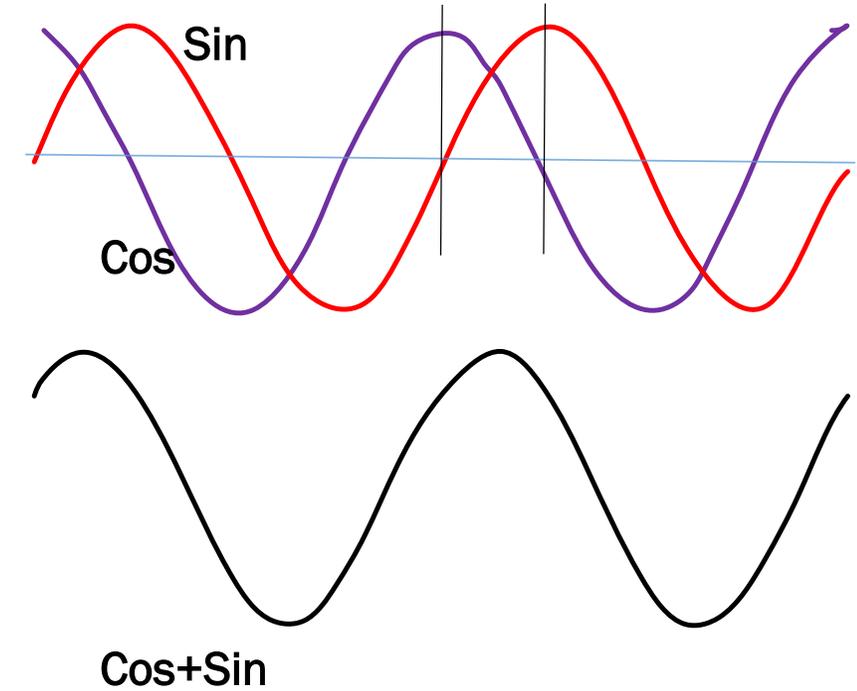
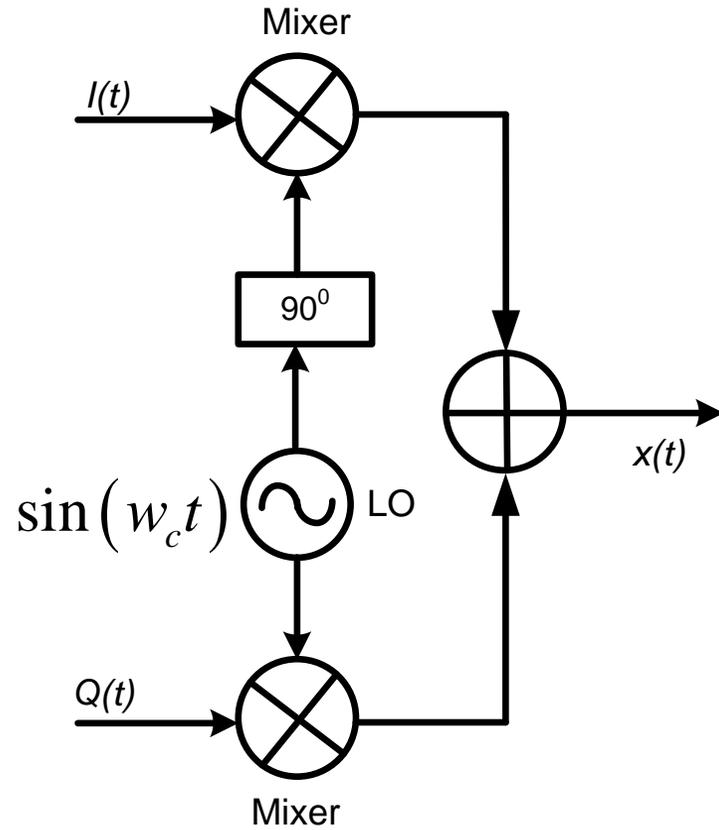
Frequency mixer

- Using Input and LO (two signals)are applied to a mixer, yields new signals at the sum and difference of the original frequencies in ideal mixer.
- Other frequency components may be present in a practical mixer.
- Used to shift signals from one frequency range to another, also known as heterodyning.
- Ex: In Superheterodyne receiver is a mixer used to translate the received signals to a IF.
- Used to modulate a carrier signal in radio transmitters.



CONT....

Quadrature Modulation



In this topic we have learnt about the

✓ **SDR Hardware, Sensitivity, Selectivity, Frequency Mixer, Quadrature Modulation**

➤ **Next we are going to Super-Heterodyne Architecture**



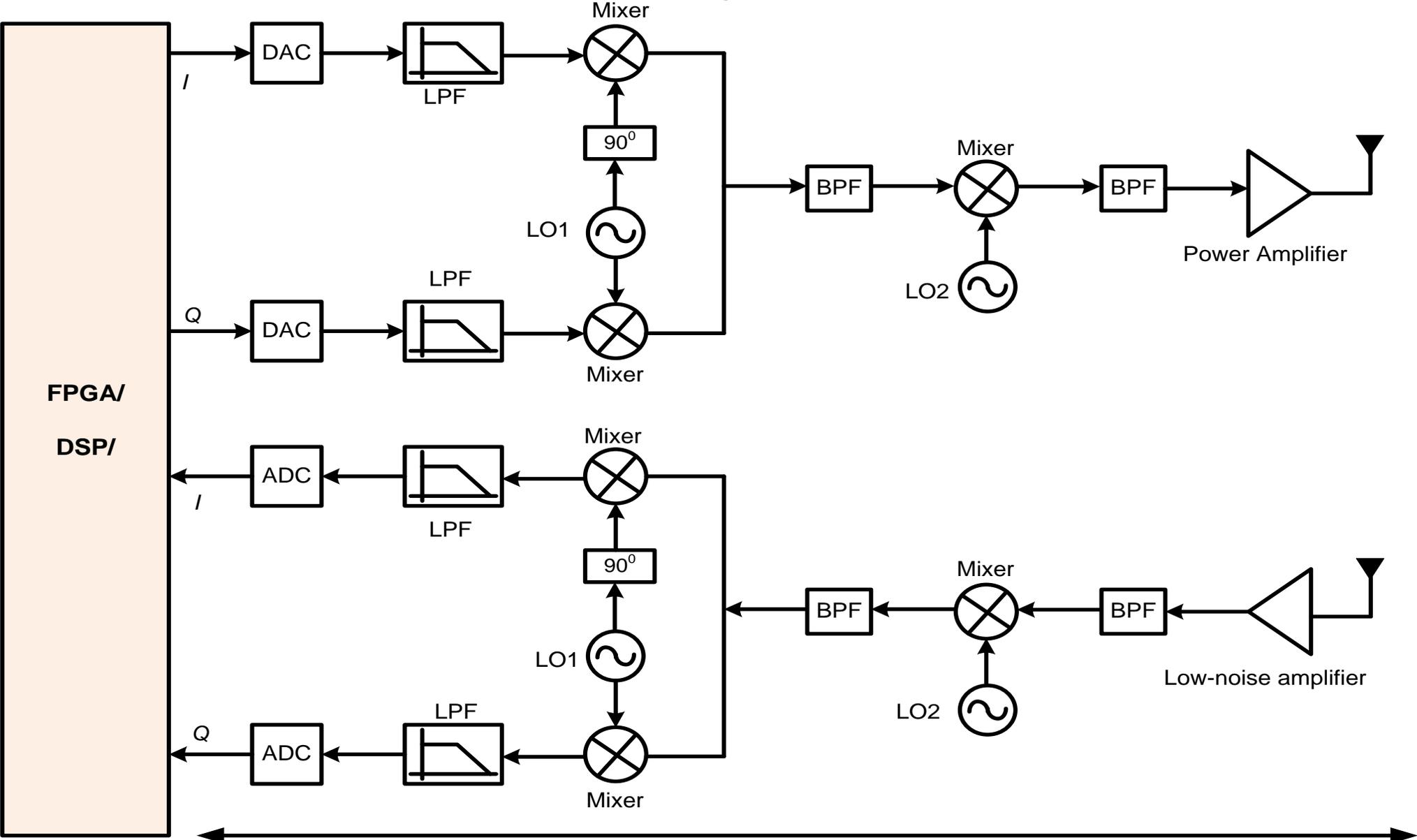
Fundamentals of SDR:RAHSDR480

Module-2:SDR Hardware Architecture

RAHSDR480_L02_P02_R01:Super-Heterodyne Architecture



Super-Heterodyne Architecture



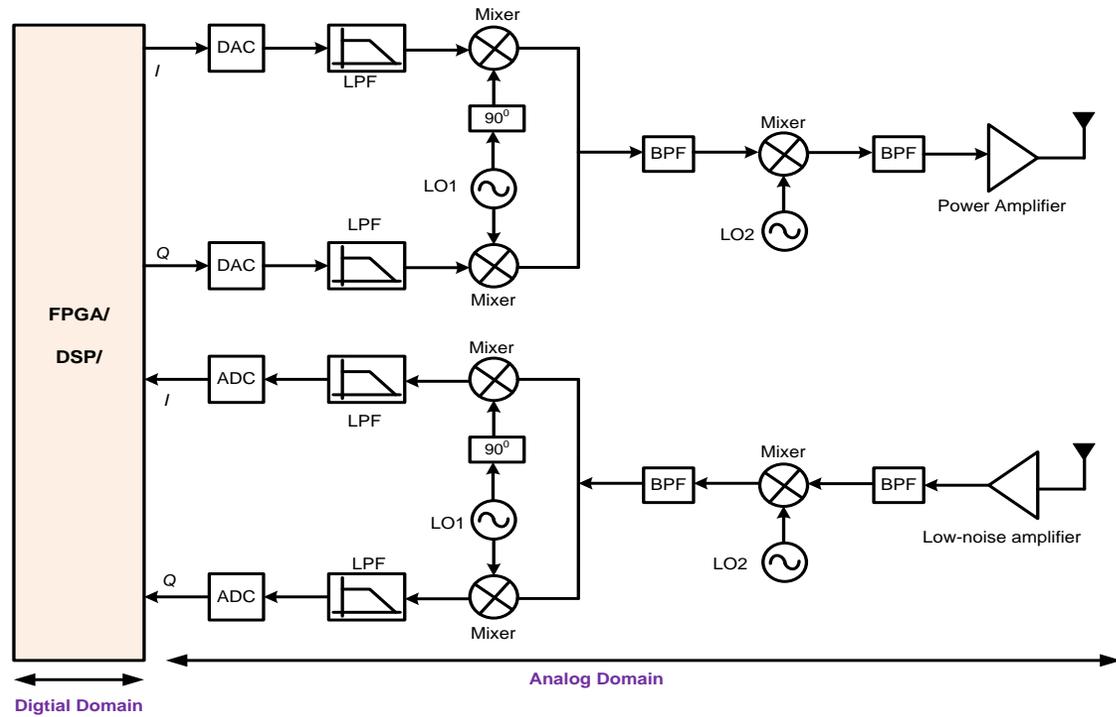
Digital Domain

Analog Domain



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CONT....



In this topic we have learnt about the

✓ **Super-Heterodyne Architecture**

➤ **Next we are going to learn Homodyne Architecture**



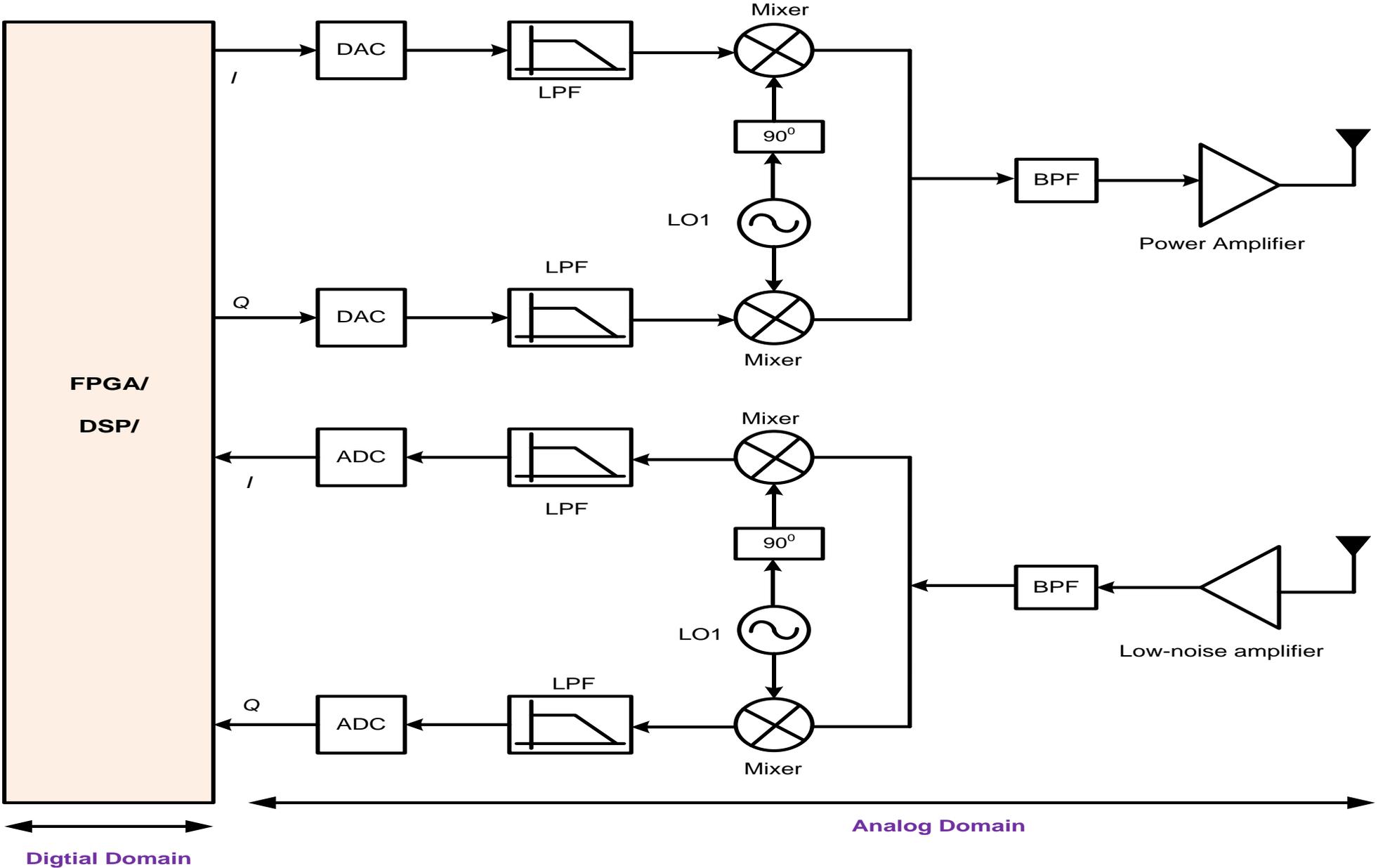
Fundamentals of SDR:RAHSDR480

Module-2:SDR Hardware Architecture

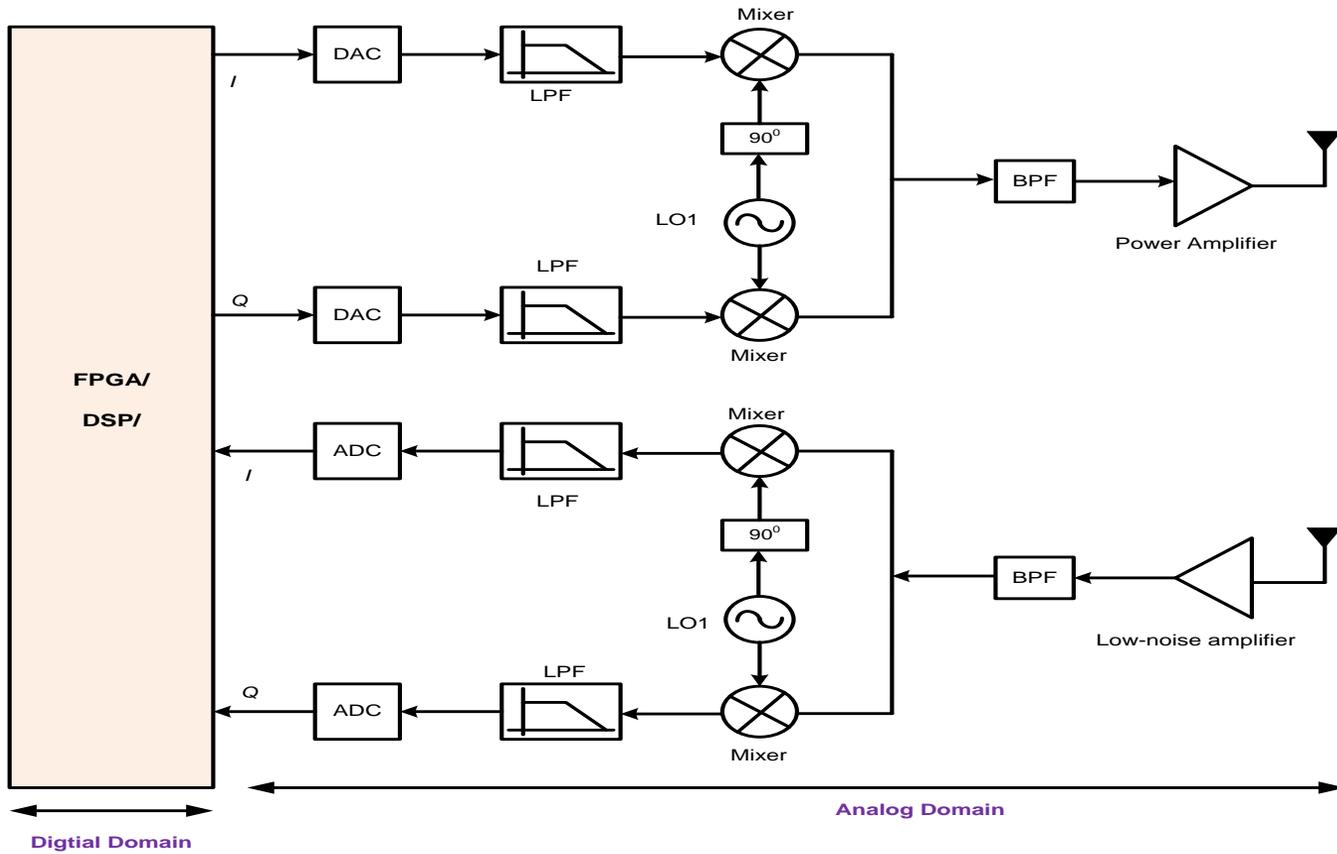
RAHSDR480_L02_P03_R01:Homodyne Architecture



Homodyne Architecture



CONT....



In this topic we have learnt about the

➤ **Homodyne Architecture**

➤ **Next we are going to learn Lo Leakage and DC Offset**



Fundamentals of SDR:RAHSDR480

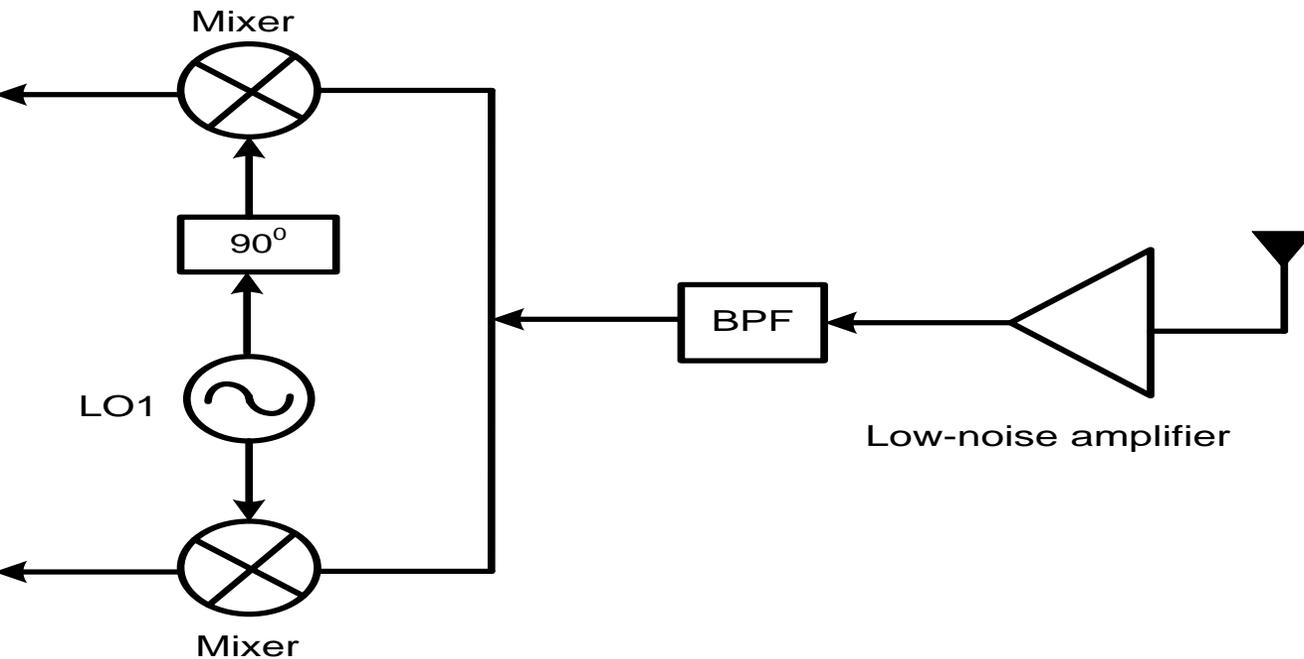
Module-2:SDR Hardware Architecture

RAHSDR480_L02_P04_R01:LO LEAKAGE AND DC OFFSET



LO LEAKAGE AND DC OFFSET

- Since LO is not perfect, there is LO leakage which causes self-mixing at mixer to produce a DC component.
- This contribute to a large DC offset due to high gain of receiving chain.



$$\sin^2 x = \frac{1 - \cos 2x}{2} \quad \cos^2 x = \frac{1 + \cos 2x}{2}$$

CONT....

Heterodyne

➤ $RF=LO1+LO2$

Homodyne

➤ $RF=LO1$



In this topic we have learnt about the

✓ LO LEAKAGE AND DC OFFSET

➤ Next we are going to learn I/Q MISMATCH OR I/Q IMBALANCE



Fundamentals of SDR:RAHSDR480

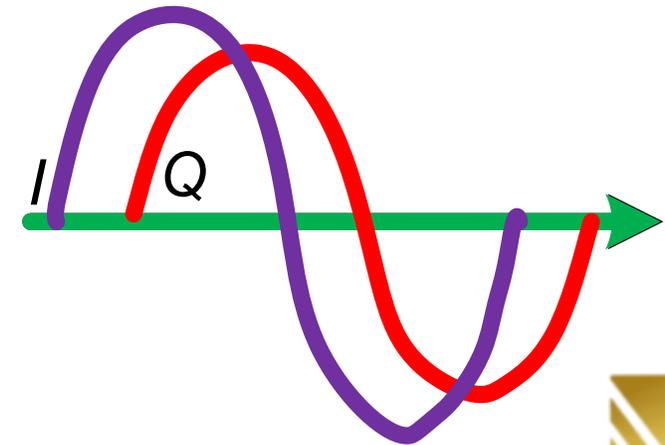
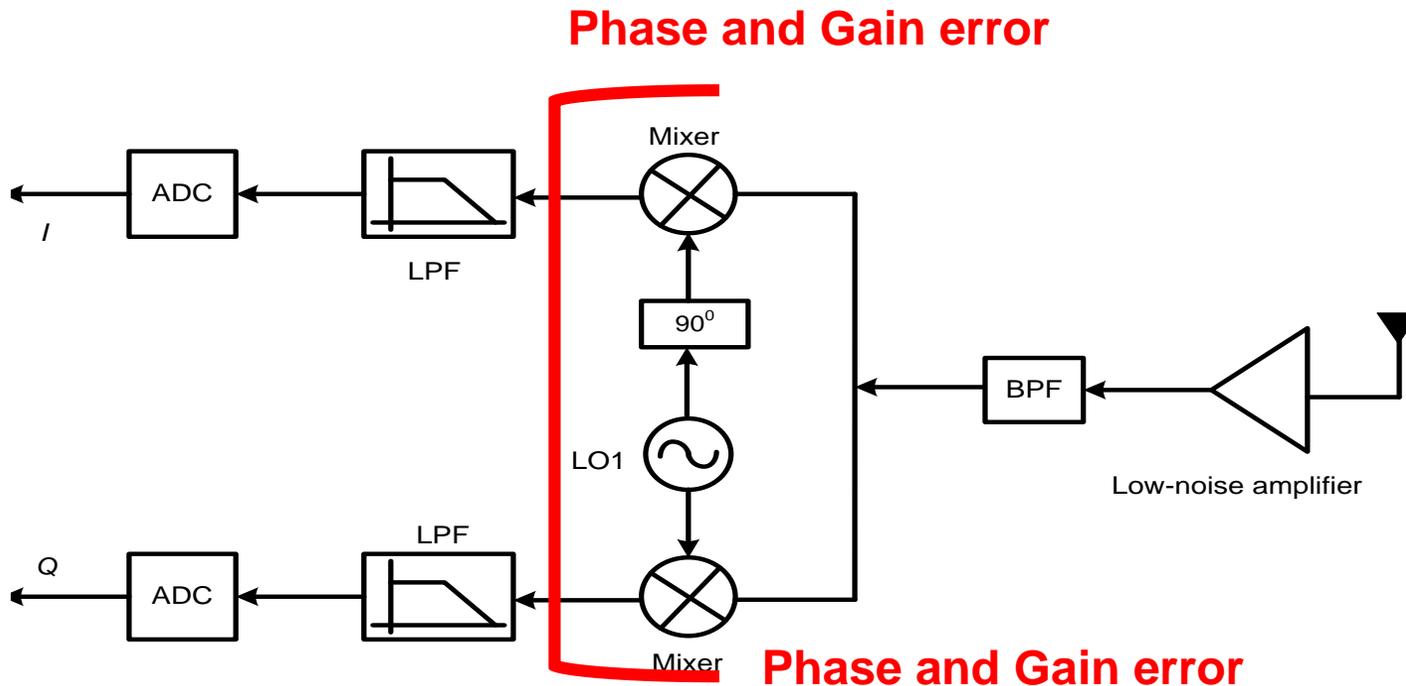
Module-2:SDR Hardware Architecture

RAHSDR480_L02_P05_R01:I/Q MISMATCH OR I/Q IMBALANCE

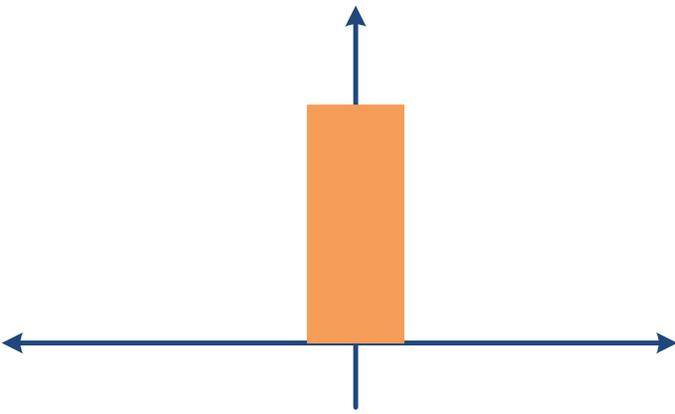


I/Q MISMATCH OR I/Q IMBALANCE

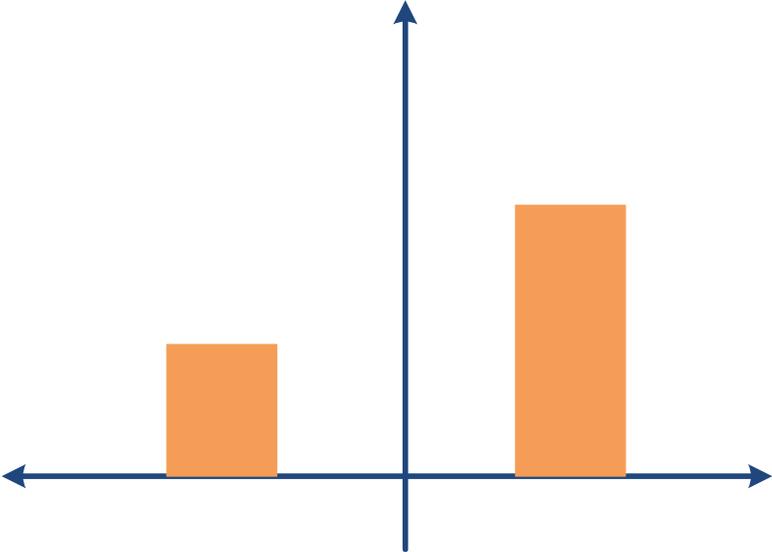
- Since the 90 degree phase shift is not ideal since it is an analog component.
- The matched pair of mixers is converting the same input signal with the dual version of the LO.
- Mismatches between the two LO signals and/or between two paths of down-conversion mixers, cause signals to be corrupted, either due to amplitude or phase differences.



CONT....



CONT....



In this topic we have learnt about the

✓ I/Q MISMATCH OR I/Q IMBALANCE

➤ Next we are going to learn HETERODYNE ARCHITECTURE

ADVANTAGES & DISADVANTAGES



Fundamentals of SDR:RAHSDR480

Module-2:SDR Hardware Architecture

RAHSDR480_L02_P06_R01:HETERODYNE ARCHITECTURE ADVANTAGES & DISADVANTAGES



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HETERODYNE ARCHITECTURE ADVANTAGES & DISADVANTAGES

➤ Advantages

- Can easily adapt itself to many different standards requirements achieving a very good sensitivity and selectivity.
- DC offset of the first few stages is removed by BPF, and that of the last stage is suppressed by the total gain in the proceeding stages.
- The LO frequency is out of the band and suppressed by BPF.

➤ Disadvantages

- Need of many external components, i.e. the image rejection filter, complexity of the structure causes problems if a high level of integration is necessary.
- It is a major drawback from the costs point of view.



In this topic we have learnt about the

- ✓ **HETERODYNE ARCHITECTURE ADVANTAGES & DISADVANTAGES**
- **Next we are going to learn HOMODYNE ARCHITECTURE ADVANTAGES & DISADVANTAGES**



Fundamentals of SDR:RAHSDR480

Module-2:SDR Hardware Architecture

RAHSDR480_L02_P07_R01:HOMODYNE ARCHITECTURE ADVANTAGES & DISADVANTAGES



HOMODYNE ARCHITECTURE ADVANTAGES & DISADVANTAGES

➤ Advantages

- Less complex and easy integration on chip.
- Easy availability of baseband signal.

➤ Disadvantages

- DC offset
- IQ imbalance



In this topic we have learnt about the

✓ **HOMODYNE ARCHITECTURE ADVANTAGES & DISADVANTAGES**

➤ **Next we are going to learn Comparison of both Architecture**



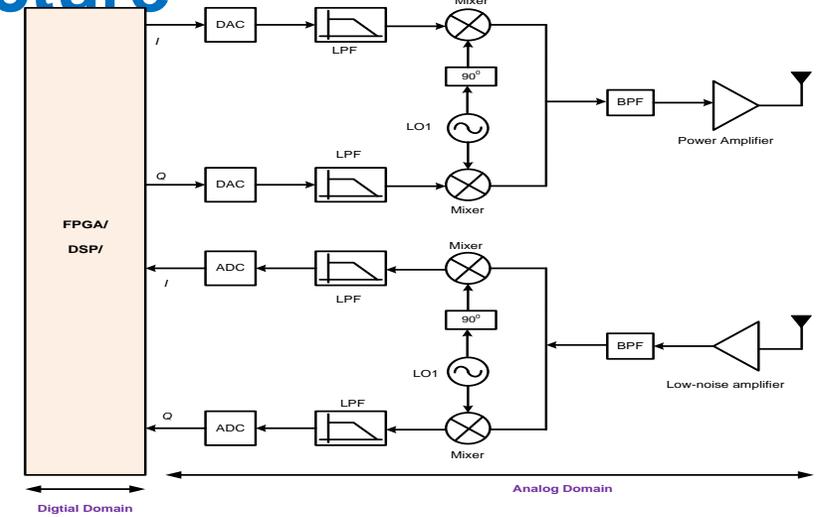
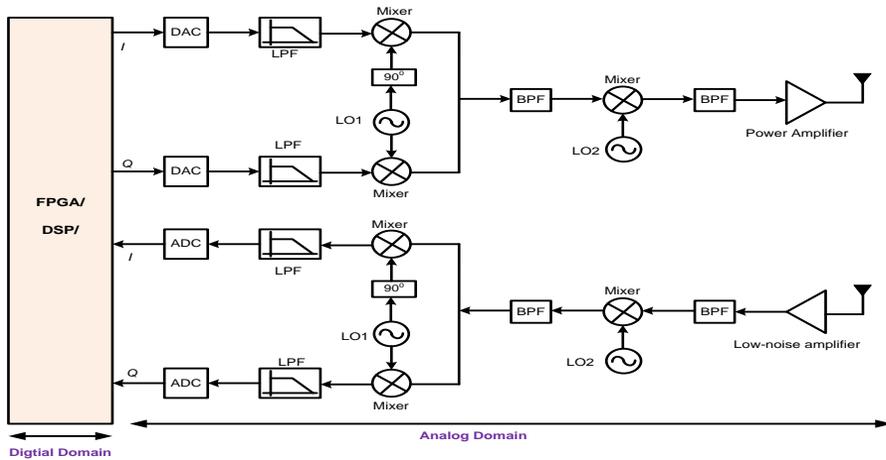
Fundamentals of SDR:RAHSDR480

Module-2:SDR Hardware Architecture

RAHSDR480_L02_P08_R01:Comparison of both Architecture



Comparison of both Architecture



- High complex, & difficult for chip based implementation.
- DC offset and LO leakage and IQ imbalance is not much significant.
- Costly due to more extra analog component.

- Easier for chip-based implementation.
- DC offset and LO leakage and IQ imbalances are very much significant.
- Less costly.



In this topic we have learnt about the

✓ **Comparison of both Architecture**

➤ **Next we are going to learn SDR Companies**



Fundamentals of SDR:RAHSDR480

Module-2:SDR Hardware Architecture

RAHSDR480_L02_P09_R01:SDR Companies-I



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SDR Companies

Analog Devices (Front-End)

ICs	Bandwidth (MHz)	Function	Frequency (GHz)
AD9361	56	2Rx, 2Tx	0.07-6
AD9364	56	1Rx, 1Tx	0.07-6
AD9363	20	2Rx, 2Tx	0.325-3.8
AD9371	100 Rx, 250 Tx, ORx	2Rx, 2Tx, ORx, SnRx	0.3-6
AD9375	100 Rx, 250 Tx, ORx	2Rx, 2Tx, ORx, SnRx	0.3-6
ADRV9009	200 Rx, 450 Tx, ORx	2Rx, (1 ORx), 2Tx	0.075-6
ADRV9008-1	200 Rx	2Rx	0.075-6
ADRV9008-2	450 Tx, ORx	2Tx, 1 ORx	0.075-6
ADRV9026	200 Rx, 450 Tx, ORx	4Rx, 4Tx, 2 ORx	0.075-6
ADRV9002	.12 to > 40	2Rx, 2Tx	0.03-6



CONT....

Front-End

Baseband

Applications

	Evaluation Boards	Carrier Platforms	
AD936x	AD-FMCOMMS2 (AD9361), AD-FMCOMMS3 (AD9361), AD-FMCOMMS4 (AD9364), AD-FMCOMMS5 (AD9361)	Xilinx® ZC706, ZC702, VC707, KC705, AC701, ZedBoard™, MITX045	3G/4G Pico cell, SDR, 3G/4G macro BTS, massive MIMO, Radar, Test equipment, Phased Array, UHF, VHF, Satellite Communication, Point-to-point communication
AD9371	ADRV9371-N/PCBZ, ADRV9371-W/PCBZ	EVAL-TPG-ZYNQ3, Xilinx ZC706	
AD9375	ADRV9375-W/PCBZ, ADRV9375-N/PCBZ	EVAL-TPG-ZYNQ3, Xilinx ZC706	
ADRV9008 ADRV9009	ADRV9009-W/PCBZ, ADRV9008-1W/PCBZ, ADRV9008-2W/PCBZ	EVAL-TPG-ZYNQ3, Xilinx ZCU102, Intel® Arria® 10 SoC	
ADRV9026	ADRV9026-HB/PCBZ, ADRV9026-MB/PCBZ, ADRV9026-LB/PCBZ	ADS8-V2EBZ, ADS9-V2EBZ, Intel Arria 10 SoC	
ADRV9002	ADRV9002NP/W1/PCBZ, ADRV0992/NP/W2/PCBZ	Xilinx ZC706 (others TBA)	

In this topic we have learnt about the

- ✓ **Analog Device based SDR**
- **Next we are going to learn other SDRs**



Fundamentals of SDR:RAHSDR480

Module-2:SDR Hardware Architecture

RAHSDR480_L02_P010_R01:SDR Companies-II



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CONT....

National Instruments

USRP-2900

USRP-2901

USRP-2920

USRP-2921

USRP-2922

USRP-2930

USRP-2932

USRP-2940

➤ Many others with frequency range from 50 MHz to 6GHz



CONT....

LimeSDR

ICs	Frequency (GHz)	Bandwidth (MHz)	Function	Duplex	Sampling Rate (MSPS)
LMS6002D	03-3.8	28	SISO	Full	40
LMS7002M	0.0001-3.8	>60	MIMO	Half and Full	ADC-160 DAC-640

Open source

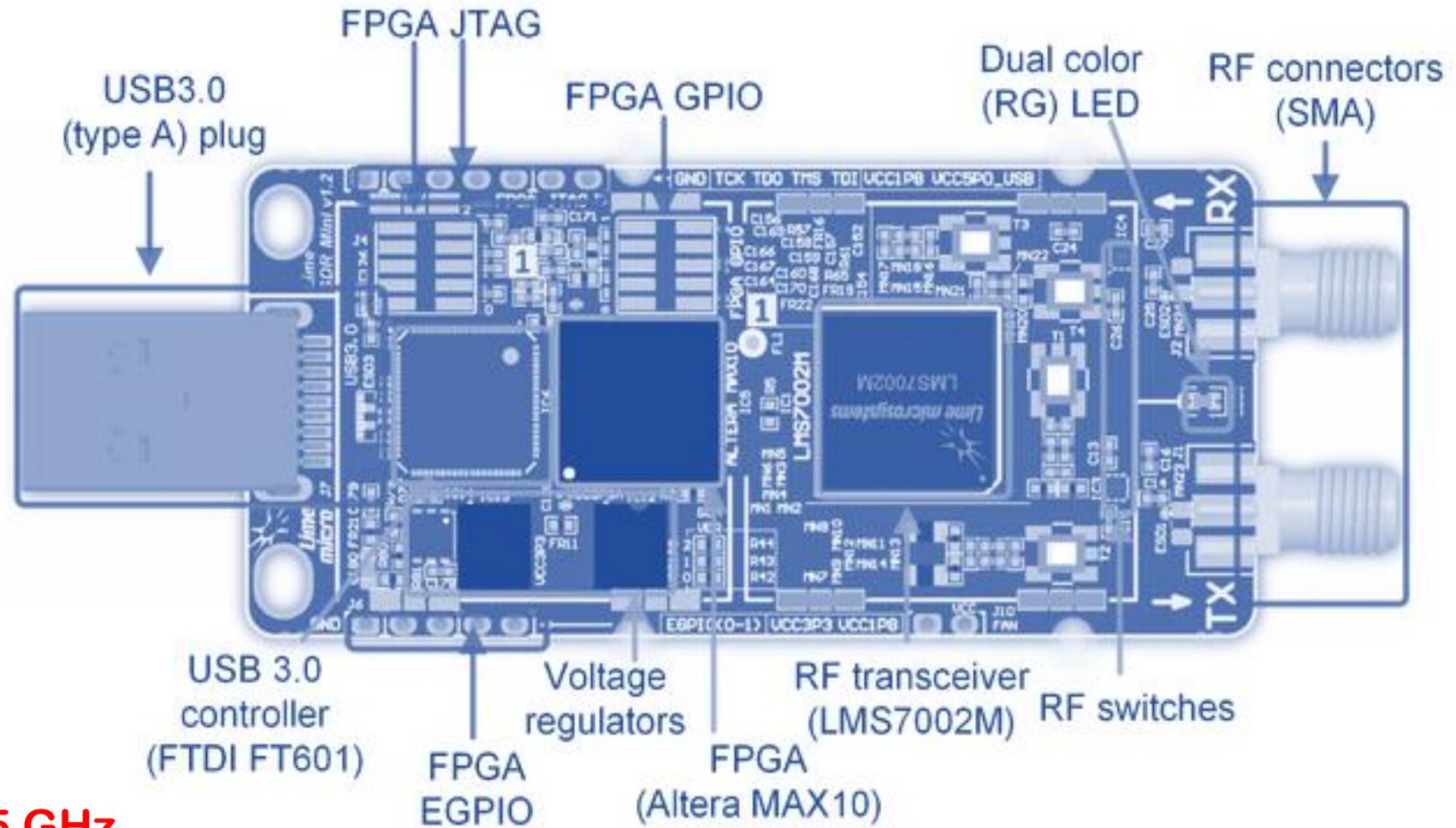
<https://limemicro.com/technology/>



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CONT....

LimeSDR



Frequency Range: 10 MHz - 3.5 GHz

RF Bandwidth 30.72 MHz

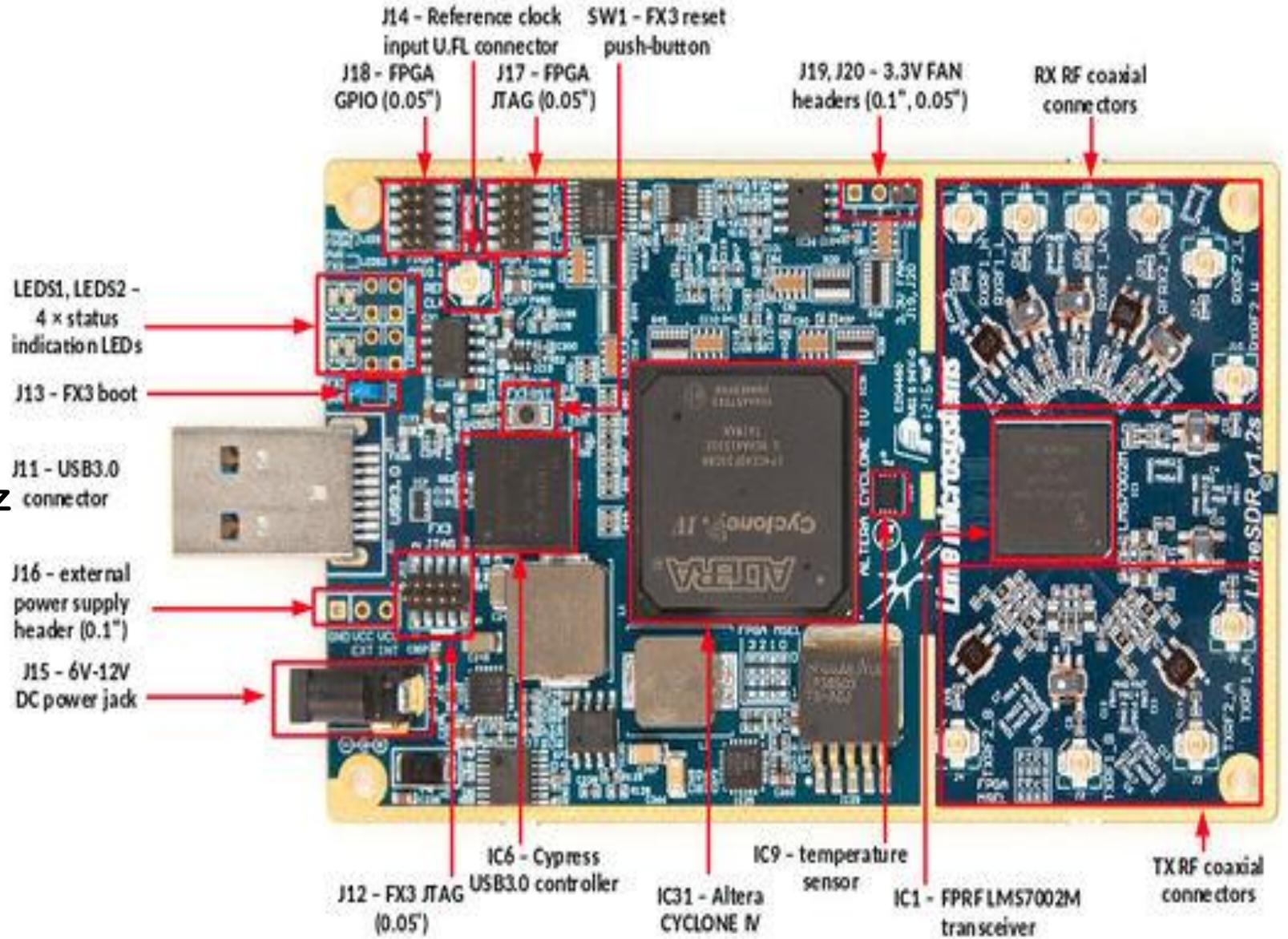
Sample Rate: 30.72 MSPS

Tx & Rx Channel: 1



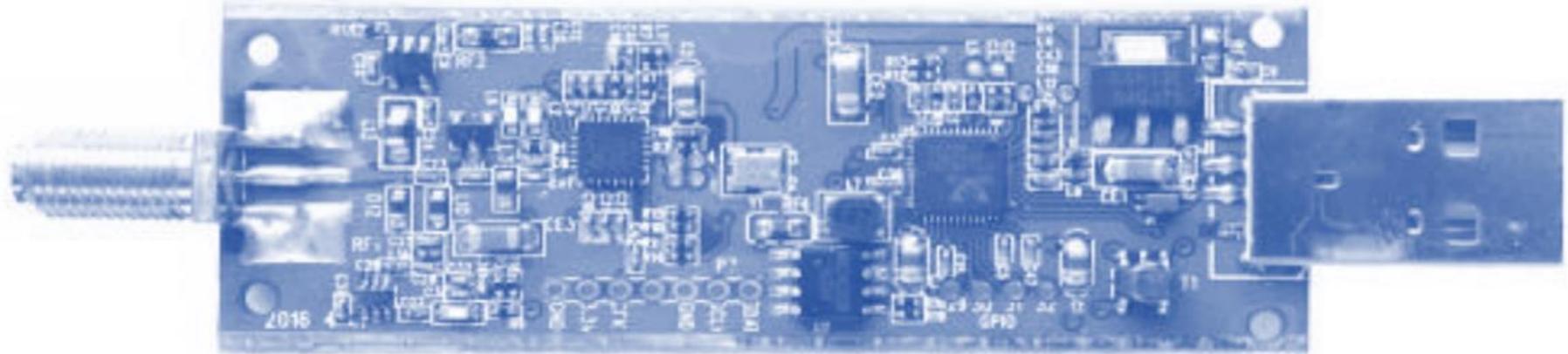
CONT....

RF Transceiver: LMS7002M MIMO
FPGA: Altera Cyclone IV
Frequency range: 100 kHz – 3.8 GHz
Bandwidth: 61.44 MHz
2x2 MIMO



CONT....

RTL-SDR



Bandwidth: Up to 2.4 MHz stable
ADC: RTL2832U 8-bits
Frequency Range: 500 kHz – 1766 MHz

<https://www.rtl-sdr.com/wp-content/uploads/2018/02/RTL-SDR-Blog-V3-Datasheet.pdf>



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CONT....

Parameters	HackRF One	Ettus B200	Ettus B210	PlutoSDR	RTL-SDR	LimeSDR
Freq. Range	1MHz-6GHz	70MHz-6GHz	70MHz-6GHz	300MHz- 3.8GHz	22MHz- 2.2GHz	100kHz- 3.8GHz
Bandwidth	20MHz	61.44MHz	61.44MHz	20MHz	3.2MHz	61.44MHz
DAC/ADC	8 bits	12 bits	12 bits	12 bits	8 bits	12 bits
Sample Rate	20MSPS	61.44MSPS	61.44MSPS	40MSPS	3.2MSPS	61.44MSPS
Tx Channels	1	1	2	1	0	2
Receivers	1	1	2	1	1	2
Duplex	Half	Full	Full	Full	N/A	Full



In this topic we have learnt about the

- ✓ **SDR Companies and their SDR systems**
- **Next we are going to do a Tear down of a SDR**



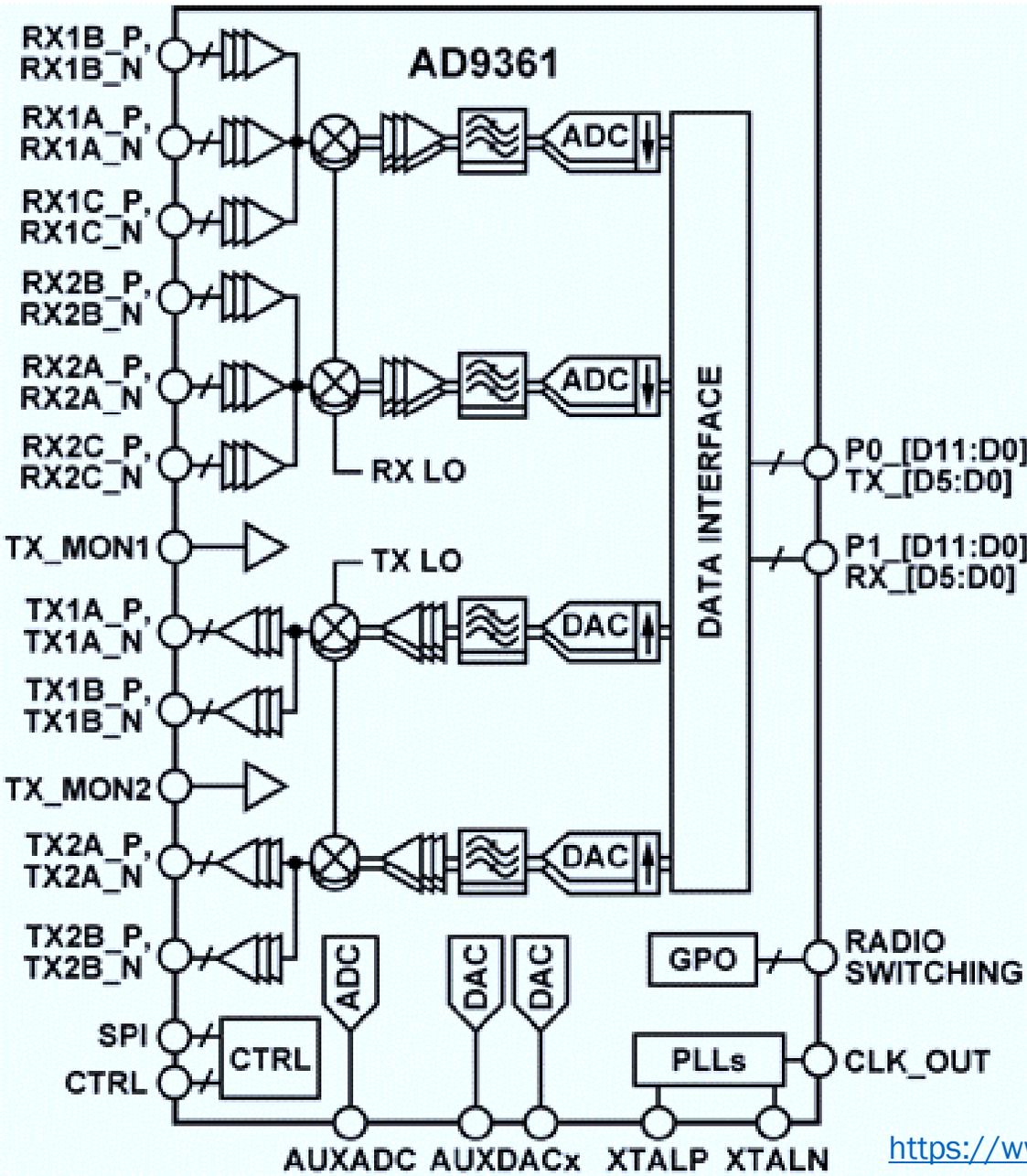
Fundamentals of SDR:RAHSDR480

Module-2:SDR Hardware Architecture

RAHSDR480_L02_P11_R01:Tear down of a SDR-I



Tear down of a SDR



- 2 × 2 transceiver
- Integrated 12-bit DACs and ADCs
- TX range: 47 MHz to 6.0 GHz
- RX range: 70 MHz to 6.0 GHz
- Tunable channel bandwidth: <200KHz to 56 MHz
- Automatic and manual gain control
- APPLICATIONS

Point to point communication systems

Femtocell/picocell/microcell base stations

General-purpose radio systems

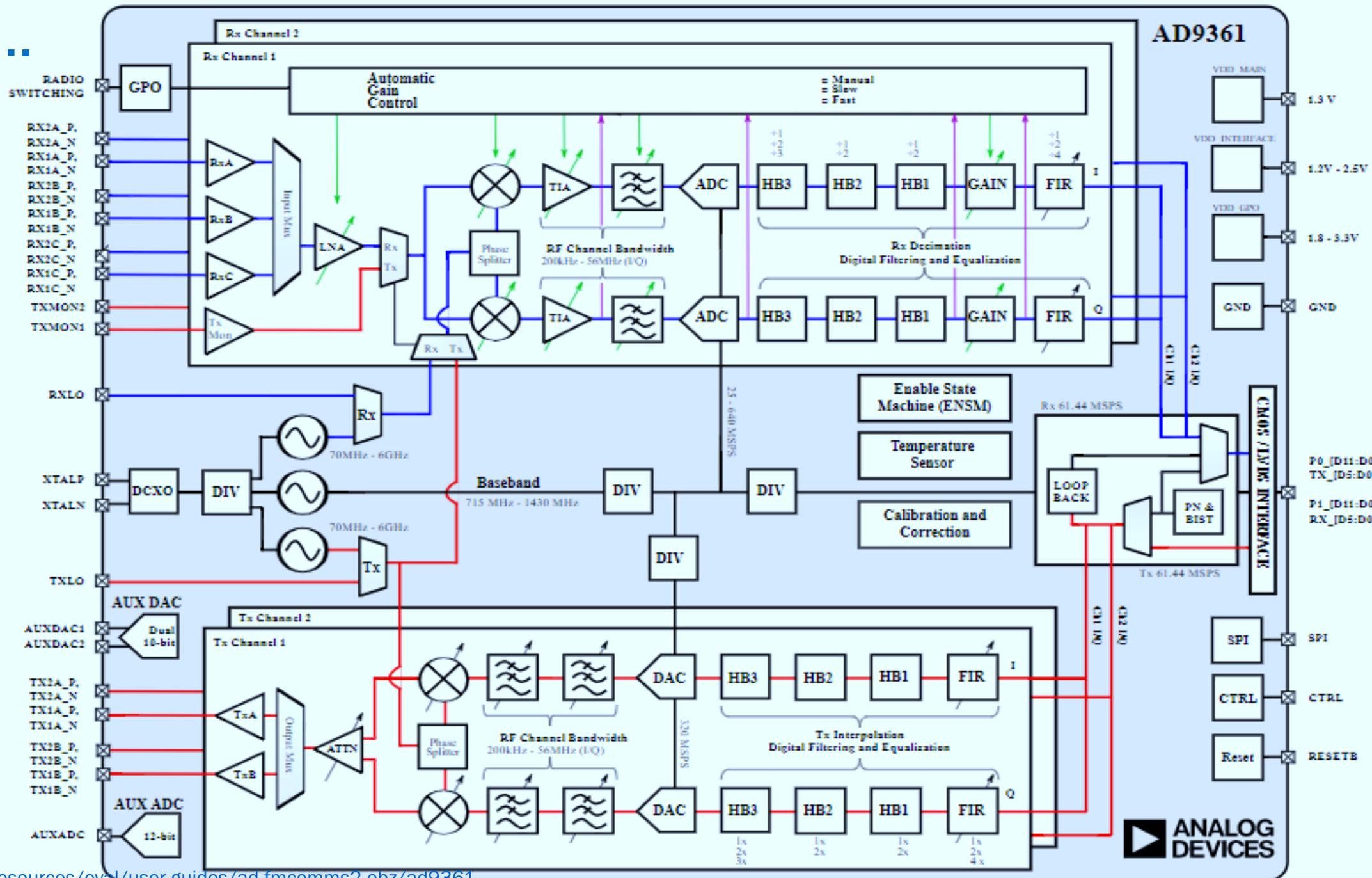
Fundamentals of SDR:RAHSDR480

Module-2:SDR Hardware Architecture

RAHSDR480_L02_P12_R01:Tear down of a SDR-II

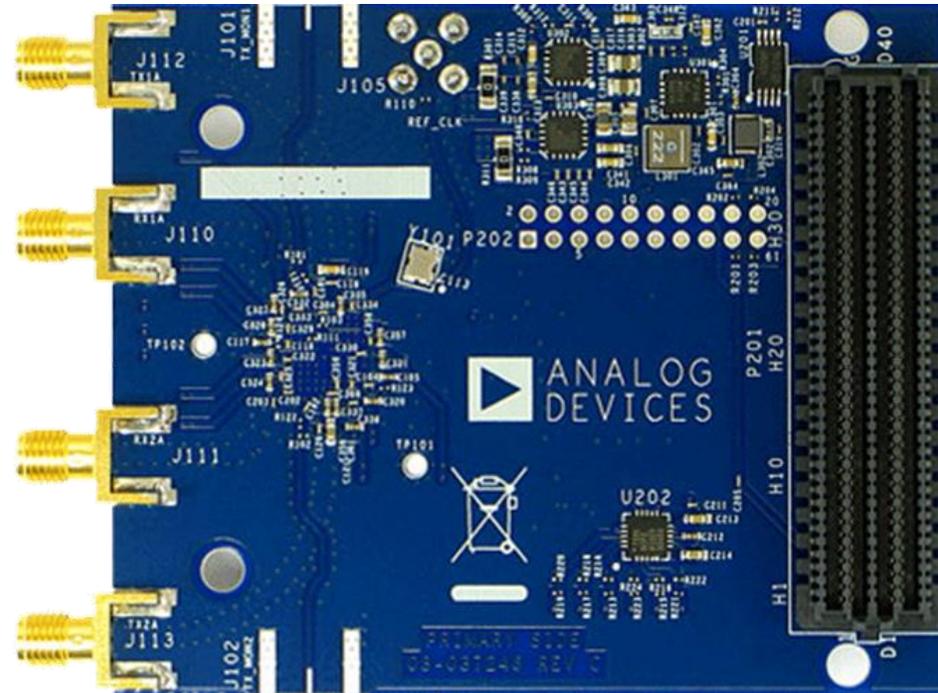
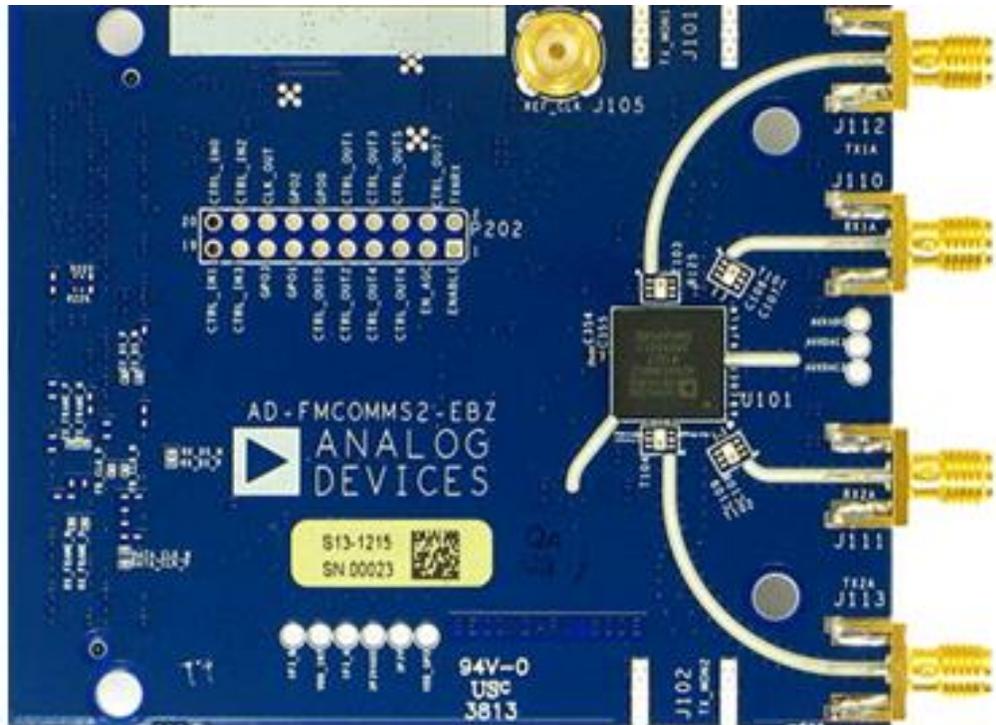


CONT....



CONT....

AD-FMCOMMS2-EBZ



RAHsoft

In this topic we have learnt about the

✓ **Tear down of a SDR**

➤ **Next we are going to learn Module-3: Communication Layer**

